AIP | Journal of Applied Physics

Study of single layer and multilayer nano-magnetic logic architectures

D. K. Karunaratne and Sanjukta Bhanja

Citation: J. Appl. Phys. **111**, 07A928 (2012); doi: 10.1063/1.3676052
View online: http://dx.doi.org/10.1063/1.3676052
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v111/i7
Published by the American Institute of Physics.

Study of single layer and multilayer nano-magnetic logic architectures

D. K. Karunaratne[a] and Sanjukta Bhanja
Electrical Engineering Department, University of South Florida, Tampa, Florida 33620, USA

(Presented 2 November 2011; received 23 September 2011; accepted 9 November 2011; published online 2 March 2012)

Nano-magnetic logic (NML) has been a promising technology for logic computation. Contribution of this paper is two-fold. First, we have fabricated and captured MFM images of a NML architecture that has computed the majority of seven variables. This logic block can potentially implement eight different logic functions that could be configured in real-time. Next, we have performed a set of experiments with a multilayer stack of $Co_{t=0.4\,nm}/Cu_{t=4\,nm}/Ni_{20}Fe_{80t=5\,nm}$ with a perpendicular magnetic anisotropy bottom layer to realize neighbor interaction between adjacent free layers of devices. Based on the MFM images, we conclude that dipolar coupling between the free layers of the neighboring spin-valve based NML (SVBN) devices can be exploited to construct local elements such as majority gates, inverters and interconnects. Since magnetic multilayer stacks have already been implemented in memory devices to read/write data, SVBN devices would not only solve the input/output problems in NML but also would have potential in logic-in-memory applications. © *2012 American Institute of Physics*. [doi:10.1063/1.3676052]

I. INTRODUCTION

Researchers are exploring novel devices/computing paradigms that will either co-exist or replace current CMOS technology since dimensional scaling of existing CMOS technology will soon approach fundamental limits. Field-coupled computing device architecture has been deemed as a potential candidate beyond-CMOS.[1] There are various versions of the field-coupled systems of computing. In this paper, the main focus is on nano-magnetic logic (NML) architecture. In NML, individual logic units are single domain magnets with shape-anisotropy. We enumerate logic 0 or logic 1 by the two possible dominant directions of magnetizations. Imre *et al.*[2] have shown an experimental demonstration of a working logical operation due to the neighbor interaction.

First, we have fabricated a seven input majority architecture using single layer nano-magnetic work, which can potentially implement as many as eight different functions, the half adder sum being one of them. All eight functions could be configured by three control parameters in real-time (by writing one or zero in them). See the schematic diagram of the 7-input majority architecture in Fig. 1(a) and SEM image in Fig. 1(b). As one can observe that there are a few ferromagnetic wires, antiferromagnetic wires, and three majority gates in the architecture. The overall logic requires 38 cells.

Even though we observed a few error-free operations, it became clear that we need better individual control and access mechanisms for successful long-term operation. Remaining part of the paper discusses a multi-layer stacked structure that (a) can potentially use low power spin-polarized current to write and clock and (b) can be read through giant magnetoresistance (GMR). Lyle *et al.*[3] have demonstrated the readability of the cells by placing magnetic tunnel junctions (MTJ) as two neighboring cells. Since the bottom layer of the MTJ was coupled with the free layer, the problem of dynamic measurements were not shown.

In this work, we demonstrate the feasibility of using such a closely spaced multi-layer stack as our elemental magnetic cell. This work is a proof of concept that the free layer of the neighboring cells would interact through dipolar coupling. Of course, this puts constraints to the bottom layer. We show in this work that *if the bottom layer is perpendicular, the free layers of the neighboring stacks interact to exhibit information manipulation and propagation.* Since MRAM technology is extremely mature and in market, we envision that this finding would be easily extended to writing and clocking through spin-polarized current and various design spaces, such as material and scaling studies, could be borrowed from the memory community keeping non-volatile logic in memory.

II. 7-INPUT MAJORITY ARCHITECTURE

In an effort to determine if indeed the NML circuits are an error free and a reliable mechanism to process and propagate information from input to output, we fabricated a complex 7-input majority architecture. This complex magnetic circuit is comprised with 38 single domain magnets with

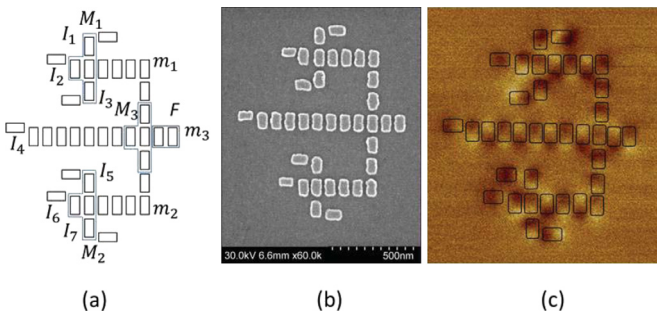

FIG. 1. (Color online) (a) Schematic diagram of the 7-input majority architecture. (b) SEM image of the 7-input majority architecture. (c) MFM image of the 7-input majority architecture.

[a]Author to whom correspondence should be addressed. Electronic mail: dkkarunaratne@gmail.com.

TABLE I. Results of the 7-input majority architecture.

Number of magnetic frustrations	0	1	2	More than 2
Number of images captured	5	6	2	5

dimensions of 100 nm × 50 nm × 5 nm and 20 nm apart from each other (see Fig. 1(b)). Previously designed and tested 3-input majority gates,[2] ferromagnetic and antiferromagnetic wires[4] have been used to design the 7-input majority architecture. The architecture is designed such that the information processing magnets have the same latency, and the system would ease to an energy minimum such that the output magnet will compute the majority of the seven variables.

The 7-input majority architecture consists of seven input variables (I_{1-7}), three 3-input majority gates (M_{1-3}), and a fanout (F) circuit. The architecture is designed to operate in two levels. In the first level, it computes the majority (m_1) of inputs I_{1-3} and majority (m_2) of inputs I_{5-7}. In the second level, it computes the majority (m_3) of inputs I_4, $m_{1,2}$ where m_3 is the majority of all seven input variables (see Fig. 1(a)).

The NML Permalloy sample was fabricated by means of electron beam lithography, e-beam evaporation, and a lift-off process. An external magnetic field was provided for stimulus and then removed. Afterwards, the system was allowed to settle to an energy minimum. The magnetic force microscopy (MFM) image in Fig. 1(c) shows no frustrations and perfect magnetic alignment in all the cells. In this experiment, we have provided all 7-inputs with logic 1, and the NML system has calculated logic 1 as the output, which is the expected correct output. To verify the reliability of computation the above experiment was repeated number of times. The errors in the computation (7-input majority architecture) was categorized into the number of magnetic frustrations. The results collected from each experiment are given in Table I. Most of the magnetic frustrations occurred in the wires and at the inputs. To minimize these errors, we have moved to multilayer NML systems for better control over individual cells.

The 7-input majority architecture can be viewed as a re-configurable hardware device. The hardware may be magnetically configured to suit a particular application/logic function. The ability to reconfigure hardware is useful and cost effective for more than prototyping simple devices. If the second (middle) input of a 3-input majority gate[2] is set to binary logic 1, it functions as a AND gate, and likewise if the input is set to logic 0, it functions as an OR gate. By simply fixing the binary states of inputs I_2, I_4, and I_6 of the majority gates M_1, M_2, M_3 respectively, to either logic 0 or 1, we can program the 7-input majority architecture to work in eight different hardware configurations. If the input variables are A, B, C, and D, the re-configurable 7-input majority architecture works as [A·B + C·D], [A + B · C + D], [A + B + C·D], [A + B + C + D], [A·B + C + D], [A + B · C·D], [A·B · C·D], [A·B · C + D]. If the input variable C = Á and B = D, the architecture could be configured to function as a XOR or as the sum of a half-adder circuit.

The inputs used in this work are set by external magnetic fields and cannot be programmed independently; different input combinations are realized by different physical arrangements of input magnets. To address this problem, we have come up with a spin-valve based NML (SVBN) device. The main intention of moving from single layer to multilayer NML is to achieve precise control (read/write/clock) over individual magnetic cells. However, the design layout of a 3-input majority gate, ferromagnetic and anitferromagnetic wire architectures would not change from single layer NML to multilayer NML.

III. SPIN-VALVE BASED NML DEVICE

The SVBN device we have demonstrated has a bottom layer with a perpendicular magnetic anisotropy, a spacer with nonmagnetic conducting metal and a free layer with an in-plane magnetization to switch its magnetic moment according to neighbor interaction. We have chosen the bottom layer to have an out-of-plane magnetization to minimize the magnetic coupling with the free layer. Spin torque transfer (STT) current would be used to write and clock the SVBN (see Fig. 2).

Fabrication of the SVBN sample involves a standard electron beam lithography process. A Hitachi SU-70 scanning electron microscope (SEM) retrofitted with the Nabity NPGS system operating at 30 kV was used to expose the patterns on a Silicon wafer with a single layer of 950 polymethyl methacrylate (PMMA) resist. Thin films of cobalt, copper, and permalloy were evaporated using a Varian model 980-2462 electron beam evaporator (EBE). A second silicon wafer was placed in close vicinity to the patterned sample in the EBE chamber for x-ray reflectivity (XRR) measurements of the multilayer sample. For the XRR measurements, a PANalytical's X'Pert PRO materials research diffractometer was used. For topological measurements and magnetic characterization, a Hitachi SU-70 SEM and a VEECO DI3000 scanning probe microscope were used.

The SVBN structure comprises a bottom layer with a perpendicular magnetic anisotropy, a spacer, and a free layer with an in-plane magnetic anisotropy. To obtain a perpendicular magnetic anisotropy, the SVBN structures were fabricated on a silicon wafer with a lattice orientation of <100>. The substrate temperature was 50 °C. A thin layer of cobalt was

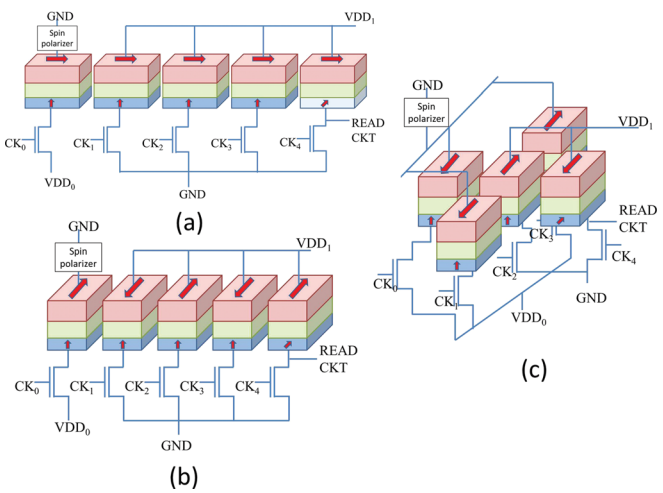

FIG. 2. (Color online) Schematic diagram of spin-valve based NML architectures. (a) Ferromagnetic wire architecture. (b) Antiferromagnetic wire architecture. (c) Majority gate architecture.

TABLE II. XRR results of the multilayer thin films.

Material	Density (g/cm^3)	Thickness (nm)	Roughness (nm)
$Ni_{20}Fe_{80}$	8.681	5	0.2
Cu	8.96	4	0.2
Co	8.9	0.4	0.1
Si	2.33	Substrate	0.1

evaporated at a rate of 0.1 Å/s in an ultrahigh vacuum chamber. The slow growth rate and the thermal energy encouraged a high quality cobalt epitaxial to have a <100> crystal lattice resulting in a high magnetocrystalline anisotropy energy[5] in the out-of-plane direction. This created the bottom layer in the stack to have a perpendicular magnetic anisotropy. Next, a thin layer of copper was deposited with a rate of 0.2 Å/s to function as the spacer of the stack. Finally, as for the free layer, a thin layer of permalloy was evaporated with a rate of 0.2 Å/s in the same vacuum chamber. Permalloy was chosen due to the fact that it has a very low coercivity and thus its magnetization is easily susceptible to change in the in-plane direction. Table II and Fig. 3 shows the XRR result of the thickness and the roughness of each layer in the stack. The lateral dimension of the stack is approximately 100 nm × 50 nm.

We have fabricated closely placed SVBN devices in the arrangements of ferromagnetic wire, antiferromagnetic wire, and a 3-input majority gate (similar to Fig. 2). The main intention of this experiment was to make observations for a proof of concept that the top/free layers would have neighbor interaction and would compute the correct output.

Figures 4(a), 4(c), 4(e), and 4(g) showed the topological SEM image of the 4- and 8-cell SVBN ferromagnetic and antiferromagnetic wire architectures. An external out-of-plane magnetic field was provided for stimulus and then removed. Afterwards, the system was allowed to settle to an energy minimal. The MFM images in Figs. 4(b), 4(d), 4(f), and 4(h) showed the top/free layers of the SVBN systems have no frustrations in them, meaning the ferromagnetic wires and antiferromagnetic wires have propagated the correct information from one end to the other. Next, we fabricated SVBN majority gate architecture. The gate was constructed with four SVBN devices aligned in ferromagnetic and antiferromagnetic coupling such that the center cell's top/free layer would switch to an energy minimum state. By varying the driver cell position, we provided a logic (111) input to the system. Figure 4(i) showed the topological SEM image of the majority gate.

An external out-of-plane magnetic field was provided for stimulus, removed, and then the system was allowed to reach an energy minimum. The MFM image in Fig. 4(j) showed expected magnetic alignment of the top/free layers of the SVBN majority gate, meaning the SVBN majority gate has computed the majority of the provided three inputs.

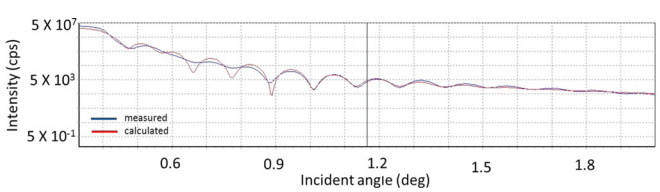

FIG. 3. (Color online) Specular-reflective curve for Si/Co/Cu/$Ni_{20}Fe_{80}$.

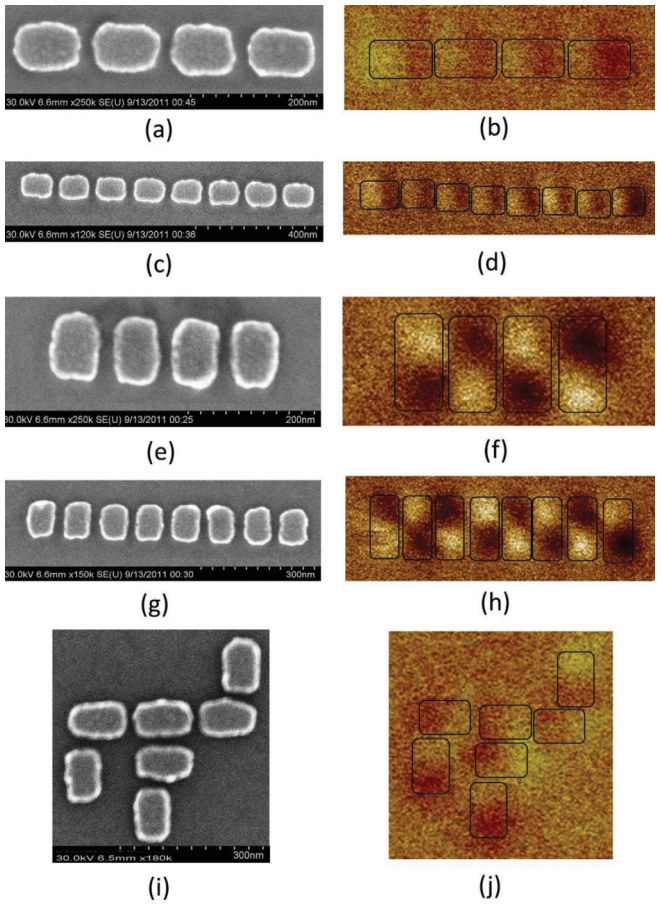

FIG. 4. (Color online) (a), (c), (e), (g), and (i) SEM images of spin-valve based NML architectures. (b), (d), (f), (h), and (j) MFM images of spin-valve based NML architectures.

The experimental observation concludes that the free layers of the SVBN devices functioned similarly to the 3-input majority gate,[2] ferromagnetic and anitferromagnetic wire[4] architectures in single layer NML systems. These exciting results can lead us to fabricate complex SVBN architectures for computing paradigms. The output cell connected to a read circuit to measure its GMR should have a bottom layer of a tilted magnetic anisotropy (see Fig. 2). Our future work is related on fabricating a patterned multilayer stack with a tilted magnetic anisotropy bottom layer and observing dipolar coupling of the free layers. These multilayer stacks achieves the goals of converting magnetic logic signals into electrical logic signals and vice versa.

ACKNOWLEDGMENTS

The authors would like to thank the Nanotechnology Research and Education Center, USF and National Science Foundation (Partial support from the NSF CAREER 0639624, NSF (CRI) 0551621, and NSF (EMT) 0829838).

[1]C. S. Lent *et al.*, Nanotechnology **4**, 49 (1993).
[2]A. Imre *et al.*, Science **311**, 205 (2006).
[3]A. Lyle *et al.*, Appl. Phys. Lett. **98**, 092502–092502-3 (2011).
[4]J. F. Pulecio *et al.*, IEEE Trans. Nanotechnol. **PP**, 1 (2011).
[5]G. H. O. Daalderop *et al.*, Phys. Rev. Lett. **68**, 682 (1992).