Low Power CMOS-Magnetic Nano-Logic With Increased Bit Controllability

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Abstract—**Conventional magnetic logic using single-domain nanomagnets face severe challenges from power consumption, during field induced writing and clocking, and from poor selectivity over the logic cells. In this paper we report a novel CMOS integrated nanomagnetic logic architecture using Magnetic Tunnel Junctions (MTJs) as elemental cells. The integration details with $22nm$ CMOS technology is discussed and the feasibility of integration studied. The access transistors of the MTJs provide certain improvement in controllability over the bits of the logic. Increased controllability prevents unnecessary switching of the cells, as discussed in the paper, and hence saves power.**

Figure 1: Single layer single-domain nanomagnets used in conventional magnetic logic. *Logic* 0 and *logic* 1 are denoted as the magnetization along the $+x$ and $-x$ direction respectively. The easy axis is aligned along the x direction. It is the energy minimum configuration of the magnet while the hard axis which is along the shorter dimension, represents the energy maxima or unstable configuration of the nanomagnetic cell.

I. INTRODUCTION

Conventional nanomagnetic logic relies on the shape anisotropy of the single-domain single layer nanomagnets for binary information storage in the magnetic form. The shape anisotropy is rendered to the nanomagnets by patterning them into elliptical or rectangular forms. The longer dimension in the structure is termed the *easy axis* while the shorter dimension is called the *hard axis* (see Fig. 1 for elliptical single layer nanomagnets). The easy axis is the energy minimum configuration of the magnetization of the nanomagnet and hence is the stable orientation of the magnetic cell. The hard axis is the energy maxima configuration and separates the two easy axes orientations by a potential barrier. The magnetization along the hard axis is therefore not stable and is inclined to settle along any of the two easy axes directions depending on the resultant field acting on it. Therefore, for switching between the two easy axes directions, sufficient energy should be provided to the nanomagnet to climb the potential barrier. Traditionally, this energy was supplied by external magnetic fields generated from overhead or underneath current carrying wires.

For information propagation and logic computation the cells need to be clocked initially. Clocking is achieved by aligning the cell's magnetization along the hard axis with the help of external magnetic field. On releasing the field, the cell settles along the resultant field direction from the neighbors. However, the current requirements for the generation of external magnetic fields is high, in the order of few mA [1], and therefore, accounts for large power consumption in the peripheral circuits. Further, the fields generated by the wires cannot be confined to only particular set of cells and hence the nanomagnetic logic suffers from stray field effects that put to question the reliability of the logic.

Devising low power logic with better control over the cells and with increased density of logic has been the key motivation behind this work. Increasing the logic density helps save area and power by minimizing redundant clocking and switching of cells. We have proposed in this paper the use of multi-layer

spintronic devices, named Magnetic Tunnel Junctions (MTJs), as the elemental cells of the nanomagnetic logic. The devices consist of two ferromagnetic layers separated by an MgO tunneling barrier. Of the two layers, one behaves as a hard magnet in the magnetic field of interest and is called the *fixed* or *reference* or *pinned* layer. The other layer behaves as a soft magnet and is referred as the *free* layer (see Fig. 2). The free layer behaves like a single-domain nanomagnet with two bistable magnetization states. The easy and hard axis of the free layer are shown in Fig. 2. The magnetization of the pinned layer is oriented in the x - z plane making an angle of $45°$ with both the x and z axis. *Logic* 0 and *logic* 1 are referred as the magnetization of the free layer along the $+x$ and $-x$ directions. The dimensions of the free layer of the cell used in our logic are $100nm \times 50nm \times 2nm$. The dimensions are above the superparamagnetic limit and hence permit room temperature operation of the device. The magnetization of the free layer can be switched between its two stable states with the help of a spin-polarized current through the device. The magnitude of the current and its direction decides the final switching. We have used this property in our nanomagnetic logic architecture to write into the cells. The typical currents used for writing is in the range of μA. Thus, reducing the power consumption for writing into the inputs of the logic.

The cells can be clocked by aligning their magnetization along the hard axis. This can be achieved by supplying a desired amount of current through the cell. By supplying a small read current through the cell and using its Tunnel Magnetoresistance (TMR) property, the state of the output cell of the logic can be determined. In order to supply the requisite current through the nanomagnetic multi-layer cells during each of the write, clock and read operations, the cells need to be integrated with underlying CMOS transistors.

After a brief review of the existing work in the fields of nanomagnetic and spintronic logic in Section II, we describe the elemental cell property and its behavior in Section III. The hy-

Tilted MTJs as basic computing elements
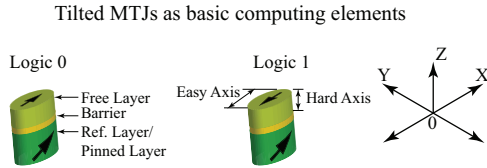
Figure 2: The free layers of the devices behave as single-domain nanomagnets. The energy minimum configuration is termed as the *easy axis* while the energy maximum is called the *hard axis*. *Logic* 1 and *logic* 0 are represented by the magnetization of the free layer along the two easy axes direction.

brid CMOS-nanomagnetic logic architecture is introduced and discussed in depth in Section IV. The characteristics of the architecture, the nomenclature of the cells constituting the architecture and the feasibility of integration of the nanomagnetic logic with $22nm$ underlying CMOS technology is focused on. An example logic flow through the architecture is also discussed in the same section. Section V describes the writing phenomena in the cell while Section VI briefly explains the clocking and the reading techniques for the architecture. Finally, Section VII concludes our work.

II. BRIEF REVIEW OF THE EXISTING NANOMAGNETIC AND SPINTRONIC LOGIC

Various experimental demonstrations of logical components like majority [2], NAND/NOR [3], AND/OR [4] have been presented for nanomagnetic logic. Performing the fundamental operations in nanomagnetic array, such as clocking the cells for state propagation, supplying inputs, and sampling computed outputs, for any complex logic implementation is a challenge due to power consumption and difficulty of integration of the underlying circuits. Clocking the magnets for perfect ordering is in general performed by field-induced clocking [1], [5], [6], [7] except in the experimental demonstration in [4] that uses a rotating magnetic field. Magnitude of current required in these clocking schemes, to generate a high enough magnetic field, is high, in the order of mA. Most of the prior works have reported static inputs and outputs observed through magnetic force microscopy. Recently, nanomagnetic systems were driven by on-chip input field current [8] where $680\ mA$ was reported for an easy axis to easy axis switching (not using clock). The experimental read-out [9] was shown by trapping domain wall of a neighboring wire. In [10] researchers have experimentally demonstrated the feasibility of integrating MTJ with nanomagnetic logic for resistance measurements.

However, as previously mentioned, clocking the cells require the assistance of external magnetic fields generated through current-carrying conductors [4], [7]. But the devices still suffer from power dissipation in the external circuits that are used for clocking. Writing to the input cells have been proposed and conducted through fields either generated by input wires external to the logic [11] or by external MTJs in close association ($1\ nm$) with the nanomagnetic cells [6]. Reading the output of the logic has been effected with the help of output sensors that transport the signal to off-chip peripherals for data determination [12]. The peripheral circuitries used in writing, reading and clocking are still a subject that has not been much explored. Feas-

ibility of simultaneous clocking and reading through the above-mentioned schemes is still an open field of study that needs further attention. Recently a group of researchers have proposed a new all-spin logic device utilizing spin transfer torque current for writing, reading and clocking the logic [13]. Logic execution involves spin injection from a ferromagnetic conductor to a semiconductor, in this case graphene. However, the injection efficiency into semiconductors is still very low and the device has not yet been fabricated.

Contrary to prior work, our study is the first effort to use multi-layer Spintronic devices as individual computing elements so that we can leverage from the *Spin Transfer Torque (STT)* induced current switching and the integration with low power CMOS while using the interaction between devices to compute and propagate information. Most importantly, this work is the first step to offer localized control over individual elements of nanomagnetic logic architecture.

## III. ELEMENTAL CELL OF PROPOSED NANOMAGNETIC LOGIC

We use MTJs with tilted polarizer pinned layers (see Fig. 2) as elemental cells of the logic. The magnetization of the pinned layers is tilted at $45°$ to the $+x$ axis and lies in the x-z plane. The free layer of these devices have their stable magnetization configurations along the $+x$ or $-x$ direction and which are referred as *logic* 0 and *logic* 1 respectively. When the device stores a *logic* 0, electrons with polarity along the $-x$ direction can travel easily through the device while electrons with opposite polarity are highly scattered [14]. When a *logic* 1 is stored, electrons of both polarities are equally scattered. This phenomenon generates a difference in resistance between the two logic states that is defined by TMR. We use this property to read the output of the logic by injecting small read current.

In our architecture, switching between the two states of a cell can take place either through STT current of suitable magnitude and direction or through magnetic interaction between the neighboring cells. For a successful switch to occur, sufficient energy should be supplied to the cell to surmount the potential hill separating its two easy axes configurations. The magnetic interaction from neighboring cells is however not sufficient to cause a switch by itself at room temperature. To assist in switching, the magnetization of a cell is therefore taken to the hard axis i.e. on top of the potential hill. This is an unstable configuration and hence the slightest resultant force from the neighbors now switches the cell to the desired logic state. This phenomenon of providing requisite energy through external means to force the cell's magnetization along the hard axis is called *clocking*.

IV. HYBRID CMOS-NANOMAGNETIC LOGIC ARCHITECTURE

A. Architecture Geometry & Cell Classification

In this paper we propose a hybrid CMOS-nanomagnetic logic architecture. The logic computation and information storage takes place in the MTJs that make the elemental computing cells of the logic. The MTJs are arranged in a regular 2D grid except for the locations that are required for the intended logic imple-
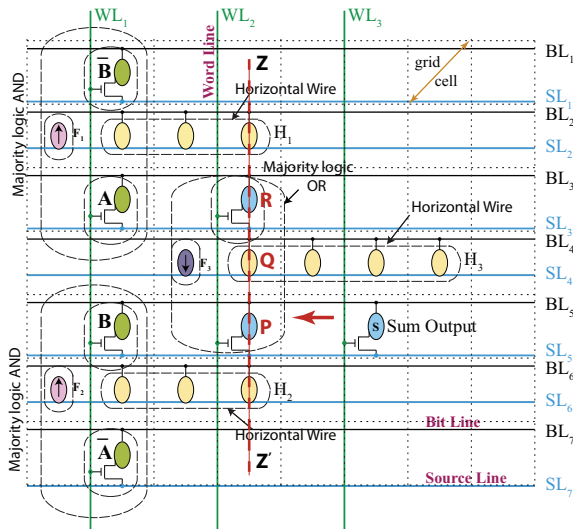
Figure 3: Generic Logic Brick for hybrid CMOS-nanomagnetic logic architecture. Dotted lines show the 2D grid with one MTJ per grid cell. Vertical word lines connect all gates of the access transistors that are in that column. Every row has a dedicated source and bit line.

Figure 4: Cross-section view along z-z′ (Fig. 3) of three vertically located cells P, Q and R, of the CMOS-nanomagnetic logic architecture seeing in the direction of the red arrow.

mentation. The 2D grid is shown by the dotted lines in Fig. 3 with a MTJ placed at the center of each grid cell. For the MTJ footprint of $100nm \times 50nm$, the separation between two MTJs is limited to $20nm$ along both the horizontal and vertical directions for effective interaction between the two free layers to take place. Therefore, the horizontal and vertical pitches of the grid are restricted to $(50 + 20)nm = 70nm$ and $(100 + 20)nm = 120nm$ respectively.

Placement of a CMOS transistor, in $22nm$ technology, underneath each MTJ cell is again limited by the metal pitches of the CMOS technology. The transistor to be integrated with a MTJ device should have sufficiently large aspect ratio to have the required current sourcing ability. Therefore, in order to build a nanomagnetic logic architecture that satisfies the constraints of nanomagnetic grid pitch, CMOS metal layer pitch and CMOS current sourcing ability, the placement of CMOS transistors has to be restricted to one for every 2×2 grid cells. A high W/L ratio also reduces the transistor's *ON* resistance.

The architecture therefore has the following categories of cells:

- **Input Cells**. These cells are at the input of the logic and are therefore only written into with the help of STT current. Each of the Input Cells has an access transistor integrated to it. The access transistor helps to increase the selectivity of the cell to the current flow through it. This helps to retain the state of the cell and hence reduce the overall power consumption of the logic by preventing unnecessary switching of these cells when the rest of the cells in its row are clocked with a STT current. These cells are marked in green (*e.g.* A, B , $\overline{A}$ & $\overline{B}$) in Fig. 3.
- **Cells in the body of the logic**
  - **Standard Cells**. These are MTJs without an access transistor. These cells are marked in yellow in Fig. 3. Standard Cells can be placed in adjacent lattice sites of the grid and their pitch is equal to the grid pitch. Whenever
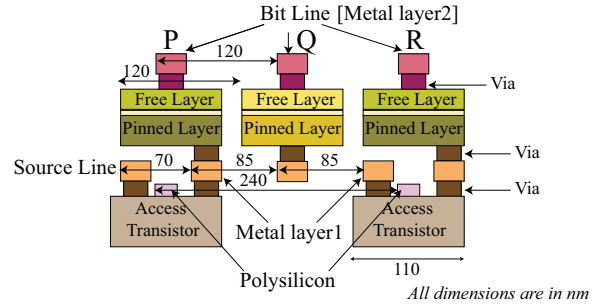
a potential difference is applied across the bit and source lines of its row, an appropriate current flows through these cells.
  - **Controlled Cells**. These are MTJs with an access transistor and are present in the body of the logic. They are marked in blue. These cells lie at the intersection of a source and bit line pair with that of a word line. These cells can only be placed in alternate lattice sites owing to the pitch restriction imposed by their access transistors. Controlled Cells reduce the overall power consumption of the logic by only switching when required during the logic computation or information propagation. By not selecting the word line of their access transistors, these cells can prevent the current flow through them when a potential is applied across the bit and source lines of their rows to supply current to the other cells in the row.

B. Routing of the Metal Layers in the Architecture

All the metal lines in the architecture are routed within three layers of metal. The rows in the architecture are distinguished by a dedicated pair of source and bit lines that are routed in the first and second layer of metal. The Input Cells share the same row with only the Controlled Cells. Therefore, when the Input Cells are written into, the architecture has the provision to turn off the access transistors of the Controlled Cells in order to permit the current flow only through the Input Cells.

All the cells in the logic block are placed with their free layers facing up. The bit lines are so routed that they connect to the center of the free layer of each cell in a row through a via as shown in Fig. 4. The figure shows the cross-section of the cells P, Q and R in Fig. 3, viewing in the direction of the red arrow. The source lines are placed such that they are either vertically above the source/drain of the access transistor of the Controlled Cells or are beneath the center of the pinned layer of a Standard Cell (see Fig. 4). The bit lines therefore maintain a constant pitch of $120nm$ while the separation between two source lines can vary from $85nm$, when a Standard Cell e.g. Q is placed vertically above a Controlled Cell e.g. R (see Fig. 4), to $155nm$ when the reverse placement of the two types of cells occur. The metal layer 1 pitch in the architecture is therefore $70nm$ stemming from the gap between the metals forming the source line and the metal landing to form contacts to the source and drain of an access transistor as shown in the Fig. 4. It meets the require-
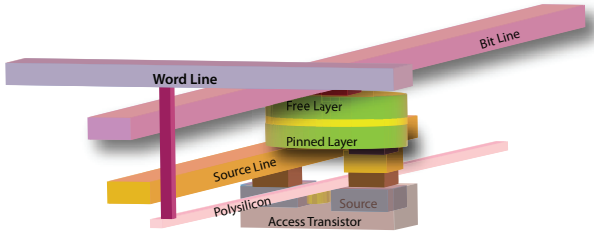
Figure 5: Controlled Cell: MTJ with access transistor. The word lines run vertically in the architecture while the source and bit lines run horizontally.

ment of $22nm$ CMOS technology where a $64nm$ metal pitch is specified by ITRS [15]. The word lines that characterize a specific column of Input Cells and Controlled Cells are routed in metal layer 3 (see Fig. 5). They are connected to the poly gates of the access transistors that are specific to that column.

C. Principle of Logic Computation in the Hybrid Architecture

In order to get the desired current through any cell of the architecture, initially a suitable potential difference is required to be applied across the corresponding bit and source lines of the row to which the cell belongs to. For a Standard Cell, this potential difference generates a current through it in accordance with its resistance. For a Controlled Cell, the complete path for the current flow takes place via the access transistor. Hence, the associated word line should also be activated to provide a current through the Controlled Cell. The switching mechanism of the cell with the help of current is discussed further in Section V. The logic computation takes place in the majority logic blocks that perform AND/OR operation depending on the state of a specific input to the logic. The value in this cell remains fixed throughout the lifetime of the logic architecture. Details of the logic blocks in the architecture is explained in Subsection D.

Information propagation takes place through the horizontal and vertical wires. In a horizontal wire (see Fig. 3), the anti-ferromagnetic coupling between the cells decide the post-clocked state of a cell. Once the clock is released, the cells tend to align to their final states in a sequential manner from the input to the output of the wire. For cells in a vertical wire the ferromagnetic coupling decides the state of a cell. The post-clock settlement again takes place sequentially from the input to the output of the wire. This ensures unidirectional information propagation through the wire. In addition, to make sure that the information in the entire body of the logic propagates in the direction from the input to the output of the logic, the cells in the immediate next clock zone remain in clocked state when the clock for the previous zone is released.

To summarize, the salient features of the architecture are:

- Regular 2D grid arrangement of MTJs with horizontal and vertical pitches of $70nm$ and $120nm$ respectively.
- A transistor for every 2×2 MTJ array.
- Dedicated Source and Bit Lines for every row and Word Line for every alternate column of the architecture.
- Anti-ferromagnetic and ferromagnetic coupling between the free layers of MTJs for effective information propagation in the wires and logic computation in the gates.

D. Constituent Logic Modules

The logic computation and information propagation in the hybrid architecture that is tailored for a specific logic behavior, takes place with the help of the following two logic modules. Some of the key aspects of the modules are discussed below:

1. *Majority logic module*: This computes a 2-input AND/OR operation by assigning the magnetization of the fixed cell to $logic\ 1$ or $logic\ 0$ respectively. Fig. 3 shows a majority AND at the input and a majority OR within the body of the logic. Please note that the pink cell in the majority AND is the fixed cell whose magnetization is fixed to $logic\ 1$. The purple cell in majority OR serves as the fixed cell. It stores a $logic\ 0$.

2. *Ferro and anti-ferro wires*: They are used for information propagation. The ferro or the vertical wires comprise of cells that are aligned parallel to their hard axes and interacts among themselves through ferromagnetic coupling. Therefore, the information at the input of the wire gets propagated unchanged to the output of the wire irrespective of the number of cells constituting the wire. The anti-ferro or the horizontal wires are built of cells that are aligned parallel to their easy axes (see Fig. 3). The cells interact among themselves anti-ferromagnetically and hence an even number of cells in the wire generate an output that is the inverted version (NOT) of the input.

E. Example Logic Flow : A Half Adder Sum Output Computation

Fig. 3 shows the cell placement for a half adder sum output generation. The Input Cells to the logic are A, B, $\overline{A}$ and $\overline{B}$ and are marked in green. The values written to the cells remain unchanged for the entire duration of a logic computation. The output is generated in cell S and is marked in blue. The rest of the cells constitute the body of the logic and are a collection of Standard Cells, marked in yellow, and Controlled Cells, marked in blue as well.

E.1 Steps of Logic Computation

We here discuss the timing steps followed to compute the Sum output, S, for the input combination of $A = 1$ and $B = 1$. Fig. 6 shows the temporal sequence of the logic computation through the different phases of the cells. The timing steps are explained below :

1. At $\mathbf{t} = \mathbf{T_0}$: Write to Input Cells, ($A = 1$, $B = 1$, $\overline{A} = 0$ & $\overline{B} = 0$) by applying required potential difference across the bit and source line pairs (BL_1, SL_1), (BL_3, SL_3), (BL_5, SL_5) & (BL_7, SL_7) and raising the word line WL_1.

2. At $\mathbf{t} = \mathbf{T_1}$: Potential difference is applied across (BL_2, SL_2) & (BL_6, SL_6) to clock the cells in the horizontal wires H_1 & H_2. Cells C and D are also clocked at the same time.

3. At $\mathbf{t} = \mathbf{T_2}$: The potential difference across (BL_2, SL_2) & (BL_6, SL_6) is released and the cells in H_1 & H_2 are left to precess and settle in accordance to the influence from the neighboring Input Cells. However, at instant $\mathbf{T_2} - \delta^*$,

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* δ is a positive quantity

Figure 6: The sequence of logic flow through the architecture during the computation of Sum Output of a Half Adder. In the figures, green represents *logic* 1, yellow represents *logic* 0, blue represents the *clocked* state of a cell. The pink and the purple cells in the figure are the fixed cells storing *logic* 1 and *logic* 0 respectively. δ and Δ are positive quantities. δ indicates the time to clock the MTJ while Δ indicates the time taken by the MTJ to precess and settle down after the clock is released. when a potential difference is applied across the bit and source lines of a row, the lines are represented by red and blue. When a word line is selected, it is shown in green. Inactive bit, source and word lines are shown in grey.

a potential difference is applied across (BL_3, SL_3) & (BL_5, SL_5) and WL_2 is raised to clock the cells P and R. The cells P and R remain in clocked state when the clock for cells in H_1 & H_2 is released. This ensures the unidirectional flow of information from the input to the output of the logic. The cells within H_1 & H_2 gets antiferromagnetically coupled to each other.

4. At $\mathbf{t} = \mathbf{T_3}$: The clock for cells P and R is released while the cells in the horizontal wire H_3 are in the clocked state by applying a potential across (BL_4, SL_4) at $\mathbf{t} = \mathbf{T_3} - \delta$.

5. At $\mathbf{t} = \mathbf{T_4}$: The clock for cells in H_3 is released and cell S is now in clocked state.

6. Finally, at $\mathbf{t} = \mathbf{T_5}$: The clock for cell S is released and the cell settles by storing a *logic* 1 in accordance to the half adder Sum logic output, $A \oplus B$.

V. WRITING TO THE INPUT CELLS

Only the Input Cells in the architecture are written into with the aid of STT current supplied by their access transistor. The access transistor dimensions should be sufficient enough to supply the requisite writing/switching current. When a current flows into the device from the free to the pinned layer the magnetization of the free layer switches to the $+x$ direction, i.e. to *logic* 0. An appropriate current in the reverse direction writes a

TABLE I: Elemental Device (MTJ) Characteristics and Switching Current Magnitudes

MTJ Footprint	$100 \times 50 \ nm^2$
Free Layer thickness	$2nm$
Horizontal pitch	$70nm$
Vertical pitch	$120nm$
Writing ($logic \ 0 \rightarrow logic \ 1$)	$278.9\mu A$
Writing ($logic \ 1 \rightarrow logic \ 0$)	$-216\mu A$

$logic$ 1 into the cell. A schematic of the Input Cell is shown in Fig. 5. The switching current magnitudes are reported in Table. I for the cell dimensions specified in the paper.

VI. CLOCKING AND READING

The clocking of the cells can be effected with the help of STT current. By providing suitable current to the cell, the magnetization of the free layer of the cell can be aligned along the y axis, i.e. the hard axis. Details of the clocking can be found in [16].

A TMR based reading technique is devised to read the output of the logic. Further details about the read circuitry is beyond the scope of this paper and interested readers are requested to refer our forthcoming publications for more details.

VII. CONCLUSION

The CMOS-nanomagnetic logic architecture is thus capable of realizing any Boolean logic function with increased controllability over the bits of the logic. This helps to reduce power consumption by preventing current flow through the cells when they are not required to perform computation. Use of current to perform writing and clocking of the cell, further reduces the energy consumption in comparison to the traditional techniques. We look forward to developing low-power peripheral decoding circuitry for this architecture in the near future.

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