Low Power Magnetic Quantum Cellular Automata Realization Using Magnetic Multi-Layer Structures

Jayita Das[1], Syed M. Alam[2], and Sanjukta Bhanja[1]

[1]Department of Electrical Engineering, University of South Florida, Tampa, FL
[2]Everspin Technologies Inc., Austin, TX

***Abstract*— In this paper, we report Magnetic Quantum Cellular Automata (MQCA) realization using multi-layer cells with tilted polarizer reference layer with a particular focus on the critical need to shift towards the multi-layer cells as elemental entities from the conventional single-domain nanomagnets. We have reported a novel spin-transfer torque current induced clocking scheme, theoretically derived the clocking current, and shown the reduction in power consumption achieved against the traditional mechanism of clocking using magnetic fields typically generated from overhead or underneath wires. We have modeled the multi-layer cell behavior in Verilog-A along with the underlying algorithm used in implementing the neighbor interaction between the cells. The paper reports the switching and clocking current magnitudes, their direction and the power consumption associated with switching and clocking operation. Finally, we present the simulation results from Verilog-A model of switching, clocking and neighbor interaction. Low power consumption due to spin transfer torque current induced switching and clocking along with the reasonable Magneto-Resistance (MR) distinguishing the two energy minimum states of the device, make these devices a promising candidate in MQCA realization.**

***Index Terms*— MQCA, Low power spin torque clocking, Nanomagnetic Logic, Non-volatile Logic, Spintronic, MTJ, Verilog-A model.**

I. Introduction

Cellular Automata involving field interaction for logic computation has been the alternative computing paradigm that offers interconnect-free design architecture, and hence, provides the scope for realizing low power circuits in the nanometer scale regime. The Quantum-dot-cellular automata (QCA), a category of Cellular Automata, uses Coulombic interaction among electrons to realize logic functionality [1], [2], [3], [4]. However, QCAs have been fabricated and functionally verified only in the cryogenic temperatures. Many interesting observations related to energy dissipation in QCA can be found in [5], [6], [7]. For example, energy dissipation increased when the tunneling energy through the clock was enhanced. Also, energy dissipation was not reduced with scaling. In fact when the cell size was 10 nm, average energy dissipation was $12\ \mu eV$ whereas energy dissipation for a 40 nm cell was calculated to be $1.8\ \mu eV$. In spite of such low energy dissipation in the computing systems, ITRS roadmap [8], reported reduced interest in Electronic-QCA due to power requirements to achieve ultra-low temperature circuit operation.

Molecular Cellular Automata and Atomic Cellular Automata are the other two offshoots of Cellular Automata involving field coupled computing. While both architectures have displayed good promise for room temperature operations, research is still under progress to develop a stable structure of the molecules [9], [10], [11], [12]. The neighbor interaction among similar cells is also a subject of study.

Magnetic Quantum Cellular Automata (MQCA), the last member of this family till date, has been the most extensively researched phenomenon that has the ability to operate at room temperature. They have been successfully employed to demonstrate various logic elements including basic logic gates and horizontal and vertical wires. The two energy minimum states by virtue of their shape anisotropy enables them to represent stable binary logic. Switching between the states takes place through an external phenomenon named Clocking. Interconnect-free low power logic has been successfully demonstrated using MQCA.

Traditionally the building blocks of MQCA logic were single-domain magnetic nanostructures [19], [13]. Clocking and the peripheral circuitries for reading from and writing into the logic were implemented using external fields that required large current densities in the wires placed below or above the cells [20]. The field, $H_{required}$ for switching a device of volume V is given by Eq. 1 where E_B represents the potential barrier between the two states and M_s, the saturation magnetization. The field generated by a current-carrying wire of radius r is given by $H_{generated}$ (see Eq. 1) where J represents the current density in the wire [21]. From the two equations it is obvious, that as the dimensions scale down, $H_{required}$ increases and to support this the current density J should increase [22], [23]. This results in large power consumption in the peripheral circuitry, that is required to supply the desired field, although the switching of the individual cells in MQCA are adiabatic in nature.

$$H_{required} = \frac{E_B}{M_s V} \qquad H_{generated} = \frac{Jr}{2} \tag{1}$$

In this paper, we therefore put forth a novel MQCA realization using multi-layer spintronic devices that are capable of being written, read and clocked using spin transfer torque (STT) current. The current requirement for each of these operations is order of magnitude lesser than the corresponding current required in field-induced operations. This along with the fact that the STT current scales down with device dimensions motivated us to use these multi-layer cells as elemental cells for nanomagnetic logic computation. We utilize interaction between the free layers of the multi-layer devices *Magnetic Tunnel Junctions (MTJs)* to compute and propagate logic information. Using STT current for writing, reading and clocking the cells provides both controllability over the individual cells in the logic and low power logic realization.

TABLE I: Experimental Demonstration of Logic Components in MQCA,$*$ indicates largest cells fabricated

Logic Implemented	Shape and minimum Size of Nanomagnets	Array Schematic	Number of cells	Input Method	Output Method
Majority Gate [13]	Rectangular; $135X70X30nm^3$		5	Through explicit neighbor magnets	Magnetic Force Microscopy
Ferromagnetic interconnect [14]	Rectangular; $100X50X20nm^3$		16	Through explicit neighbor magnets	Magnetic Force Microscopy
Antiferromagnetic interconnect [14]	Rectangular; $100X50X20nm^3$		64	Through explicit neighbor magnets	Magnetic Force Microscopy
Fanout [15]	Rectangular; $200X100X40nm^3$		16	No input, energy minimum	Magnetic Force Microscopy
Majority with lines [14]	Rectangular; $200X100X40nm^3$		9	Through explicit neighbor magnets	Magnetic Force Microscopy
Co-planar Crosswire [16]	Rectangular; $100X50X20nm^3$		10, 120*	No input, energy minimum	Magnetic Force Microscopy
NAND/NOR [17]	Rectangular; $200\ X\ 100X10nm^3$		5	Field induced	Magnetic Force Microscopy
AND/OR [18]	Rectangular; $150X60X40nm^3$		3	Through Explicit neighbor interaction	Magnetic Force Microscopy

The cell sizes are accordingly chosen to enable integration with existing CMOS technology. The integration with CMOS facilitates built-in read circuitry for reading the logic output and providing currents for clocking and writing into the cells.

After a review of the existing work in MQCA in Section II, we have studied the suitabilities and the drawbacks of various possible cell elements for implementing MQCA in Section III. We have presented a detailed theoretical analysis of a novel clocking scheme that supports low power logic computation in Section IV and the requisite of a tilted-polarizer multi-layer device for supporting the clocking mechanism is put forth. Through our discussions we have elucidated the benefits of the tilted-polarizer architecture over other multi-layer architectures and their suitability in low power logic implementation. Section V reports the first simulation model, to our knowledge, of the cell with the neighbor interaction modeled using a Finite State machine. Our classification of cell into Horizontal and Vertical Cells for generalization of the model is also discussed in the same Section along with the underlying algorithm that determines the post clocking cell behavior. Section VI reports the current magnitudes and the power consumed during each of the switching and clocking operations. The values support the implementation of low-power logic using the tilted-polarizer multi-layer stacks. Finally, Section VII concludes our report.

II. Literature Review

Extensive research has been conducted in the field of MQCA ever since its inception. The early works by Cowburn et al. [19] and Imre et al. [13] have demonstrated successful room temperature MQCA logic implementation and information propagation through ferromagnetic and anti-ferromagnetic coupling between single-domain nanomagnetic logic cells. For dimensions within the super-paramagnetic limit to the single-domain limit (i.e. $10\ nm$ to $100\ nm$), the nanocells have demonstrated successful logic operation at room temperatures. Table I outlines the logic components that were effectively fabricated along with the shape and size of individual cells, their input feeding mechanism, and mechanism of reading the output of the logic.

However, as previously mentioned, clocking the cells require the assistance of external magnetic fields generated through current-carrying conductors [18], [24]. But the devices still suffer from power dissipation in the external circuits that are used for clocking. Writing to the input cells have been proposed and conducted through fields either generated by input wires external to the logic [25] or by external MTJs in close association ($1\ nm$) with the nanomagnetic cells [26]. Reading the output of the logic has been effected with the help of output sensors that transport the signal to off-chip peripherals for data determination [27]. The peripheral circuitries used in writing, reading and clocking are still a subject that has not been much explored. Feasibility of simultaneous clocking and reading through the above-mentioned schemes is still an open field of study that needs further attention. Recently a group of researchers have proposed a new all-spin logic device utilizing spin transfer torque current for writing, reading and clocking the logic [28]. Logic execution involves spin injection from a ferromagnetic conductor to a semiconductor, in this case graphene. However, the injection efficiency into semiconductors is still very low and the device has not yet been fabricated.

We have extended the existing MQCA architecture by

TABLE II: List of symbols for equations

Symbols	Description
P	Spin-polarizing factor [29]
$\hat{s_1}$, $\hat{s_2}$	Unit vectors along the global spin orientation of the reference and free layers respectively
M_s	Saturation magnetization of the material
μ_0	Permittivity of free-space
$\|e\|$	Electron charge
α	Damping constant
γ	Gyromagnetic ratio
$\hbar$	Reduced Planck's Constant
L,W,d	Length, Width and Thickness of free layer
Vol	Volume of free layer
H_k	Anisotropy field
H_d	Coupling field from reference layer
H_{dx},H_{dz}	x- and z-components of coupling field
$\mathbf{H_{eff}}$	Effective magnetic field on the free layer arising from crystalline and shape anisotropy, demagnetization field, exchange field and external field which can be in the form of coupling from the reference layer
M_x,M_y,M_z	x,y, z-component of magnetization of free layer
$\mathbf{m}$, $\mathbf{e_p}$	Unit vector in the direction of magnetization of free and reference layer respectively
D_x,D_y,D_z	x,y, z-component of demagnetizing factor of free layer
θ	Difference in magnetization direction of free and reference layer
G_p, G_{ap}	Conductivities for fully parallel($\theta = 0^\circ$) and fully anti-parallel($\theta = 180^\circ$) states
α_p,β_p,γ_p	Direction cosines of tilted polarized reference layer

utilizing multi-layer cells MTJs to perform logic computation that offers a solution to the challenges faced by the traditional single-domain nanocells. The cells offer the ability to individually switch and clock through STT current-induced current. However, the cell sizes are limited by the super-paramagnetic and single-domain limits and the underlying CMOS technology. By choosing appropriate device architecture and dimensions, within the permissible thermal stability and single-domain limits, the switching and clocking currents can be kept in the μA range and their durations in the range of few $picoseconds$, thus improving on the power and energy dissipation faced by the earlier versions of MQCAs and simultaneously targeting towards high speed logic realization.

III. Various cell elements for MQCA logic implementation

Computing through magneto-static interaction among cells was initially carried out using single-domain nanomagnetic cells. The size of the cells gave them their single-domain property while their shape anisotropy rendered a distinct easy and hard axis to their magnetization. The magnetization of the cells always tend to align along any of the two easy-axes directions in order to be in their energy minimum state. The cells were taken to their energy maximum state (*aligned along any of their hard axes*) using an external field in the direction of their hard axes. This phenomenon was used to suitably clock the cells using an external field pulse. When the field pulse was released, the cells settled along one of their two easy axes directions under the influence of the neighboring cells. Each of the two easy axes directions were employed to represent the two different binary logic states '1' and '0'. Logic computation was carried out using suitable placement of cells with the help of external field pulse to clock them. But this approach of logic computation using single-domain nanocells faced serious challenges in their ability to demonstrate individual control over cells during clocking. Therefore, a group of cells always required to be clocked together, hence, demanding greater area for logic implementation. Moreover, the field pulses would require overhead or underneath wires and the current requirement for clocking the cells was large [20] (*in the orders of mA*). This posed a hindrance to the development of low power circuits using this approach, although the cells themselves underwent adiabatic switching. In addition, the logic implemented using such elemental devices had to rely on external circuits to write to its inputs and to read its outputs.

The basic multi-layer stacks comprised of two ferromagnetic materials separated by a barrier and are referred as MTJs in literature. While commonly employed in memory, they offer a possible solution to the challenges faced by the single-domain nanomagnetic cells. Like the single-domain cells, the ferromagnetic layers in the stack are also single domain and possess distinct easy and hard axes by virtue of their size and shape anisotropy. Their dimensions below 100nm, assists in the predominance of the spin-transfer torque effect on the devices over the magnetic field generated by the current through the device [29]. The ferromagnetic layers are so fabricated that one of them has a larger coercive field than the other that renders it a behavior similar to a hard magnet in the field of interest, while the other layer behaves as a soft magnet in the same field regime. The layer with stronger magnetization is commonly referred to as the *fixed layer* or *pinned layer* or *reference layer* in accordance to its inclination to retain its magnetization along a specific direction while the other layer is referred as the *free layer* owing to its ability to easily switch its state of magnetization. However, these devices have the unique property to switch the magnetization of their free layer under the influence of spin-polarized current. This unique property gives individual controllability over cells during switching as opposed to field pulses wherein a cluster of cells is unavoidably switched together. The property of STT current-induced switching is captured in Eq. (2) by the additional term $\mathbf{m}\times\mathbf{e}_p\times\mathbf{m}$ to the original Landau-Lifshitz-Gilbert (LLG) equation. This term refers to the spin-torque generated by the current through the device, which either aids or opposes the damping torque depending on its direction of flow.

$$\frac{d\mathbf{m}}{dt} = -\gamma M_s \mathbf{m} \times \left(\mathbf{h_{eff}} - \frac{\alpha}{\gamma M_s}\frac{d\mathbf{m}}{dt} - \frac{J_e G}{J_p}\mathbf{e}_p \times \mathbf{m} \right) \quad (2)$$

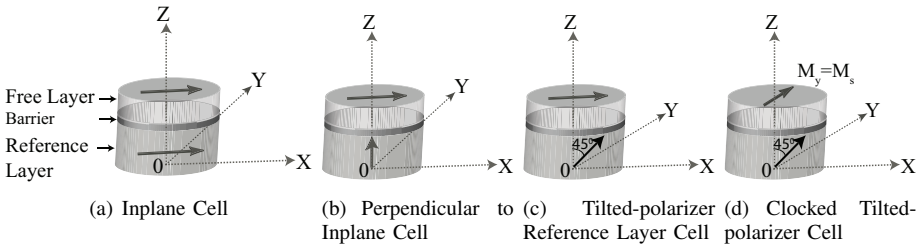
where,

$$G = \left[-4 + (1+P)^3 \frac{(3+\hat{s_1}.\hat{s_2})}{4P^{3/2}} \right]^{-1} \quad (3)$$

$$J_p = \mu_0 \cdot M_s^2 \frac{\mid e \mid d}{\hbar} \quad (4)$$

Table II defines the symbols used in the equations.

The cells are described to be in their *parallel state* or *logic '0'* when the magnetization of their free and reference layers are aligned in the same direction while they are in their *anti-parallel state* or *logic '1'* when the magnetization of their two layers are in opposite direction. A *positive current*, in the direction from the reference to the free layer, switches the cell to its logic '1' state, while a *negative current* in the opposite direction orients the cell to its logic '0' state. This



(a) Inplane Cell (b) Perpendicular to Inplane Cell (c) Tilted-polarizer Reference Layer Cell (d) Clocked Tilted-polarizer Cell

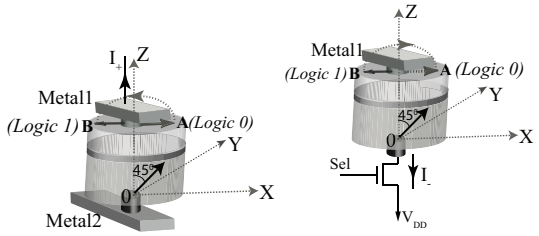
Fig. 1: Various configurations of Multi-Layer Cells. **(a) Inplane Cell:** Both the reference and the free layers have their easy axis along x-direction. Logic computation is not possible. **(b) Perpendicular to Inplane Cell:** The free layer has its easy axis along the x-direction while the reference layer has it along z which is perpendicular to the plane of the layer. Logic computation is possible but no read distinguishibility between states. **(c) Tilted-polarizer reference layer Cell:** Cells with their reference layer aligned equally to the z and x-axis while their free layer have an inplane anisotropy along x-direction. Cells are capable of using neighbor interaction for logic computation. Distinctive TMR separates the +x orientation of free layer from the -x alignment. STT current-induced low power clocking can be achieved. **(d) Tilted-polarizer Reference Layer Cell when clocked:** Low power STT current-induced clocking achieved using stationary states of the free layer aligned along y-direction.

property of switching between logic states through suitable currents (exceeding their threshold limit derived from Eq. (2)) has been effectively used to write data into the new generation memories. However, the cells need to be sufficiently distanced apart in a memory to prevent possible neighbor interaction from influencing the existing state of a cell. Once a logic state is written into the cell, the cell retains its state till the next switching current overwrites it. Therefore, these devices offer the potential to realize non-volatile logic when suitably placed so as to utilize the neighbor interaction to perform logic computation.

We realized that this neighbor interaction among multi-layer cells could be suitably used to realize low-power, non-volatile, high-speed logic capable of integrating with an underlying CMOS technology. In our effort to realize this novel thought we first attempted using a multi-layer stack that has an inplane easy-axis in both the free and the reference layers, termed as **Inplane Cell** (see Fig. 1(a)). For our convenience we have chosen the easy axis to be along the x-direction. The magnetization of the reference layer is chosen to be along the +x direction. The hard axis or energy maximum state is along the z-direction, which is perpendicular to the plane of the structure. The y-direction represents a saddle point under zero field condition. The multi-layer device can be sandwiched either directly between two horizontal wires Metal1 and Metal2 sufficiently spaced to accommodate the device (see Fig. 2(a)) or between the source/drain of an underlying MOS transistor and an overhead metal line ($Metal1$) (see Fig. 2(b)). The device is switched between its two energy minimum states by applying suitable voltage pulses across its terminals. Information propagation along a specified direction through neighbor interaction can be brought into effect by using suitable clocking technique, which assists the device to cross-over the energy barrier separating its two energy minimum states. Unlike previously reported in nanocells [19], [13], [20] we propose to use current to perform the requisite clocking, which would align the magnetization of the free layer along the y-direction (saddle points). When released, the device is expected to align along any of its easy axes directions depending on the state of the neighboring cells. However, we have observed through simulations [30] using LLG-simulation suite [31], that in such a cell the coupling from the reference layer onto the free layer has a stronger influence on deciding the state after the clock is released. Therefore, this particular cell architecture was not found suitable to effectively utilize the coupling from neighbors to propagate information.

Thereafter, we studied the device behavior of a stack with a perpendicularly polarized reference layer and an in-plane polarized free layer, termed as **Perpendicular to Inplane Cell** (see Fig. 1(b)). The logic states in such a device are represented through the two easy axes directions of the free layer. The perpendicular magnetization of the reference layer offers no inplane coupling on the free layer which places these devices in better positions to realize logic through neighbor interaction. Post clocking neighbor interaction in these devices has been verified through simulation [30]. However, it can be theoretically proven that these devices are inept to have their magnetization of the free layer oriented in the y-z plane with the sole assistance of a spin-torque current. Such a magnetization state in the y-z plane is sought after for clocking the device. Moreover, such a device configuration suffers from zero resistance difference between its two logic states and hence the inability to read the state of the output cells using any readout schemes. Use of different architectures for the outputs as in [32], [22] would result in an inhomogeneous logic implementation that would increase the cost of logic fabrication.

A device architecture with a tilted polarizer reference layer [33], [34] and an inplane polarized free layer, named as **Tilted-polarizer Reference Layer Cell** (see Fig. 1(b)), offers a solution to all the challenges discussed above. In this paper, we would refer logic '1' and logic '0' states as the free layer magnetization along the '+x' and '-x' directions respectively. Such a cell can be clocked using a spin-torque current and the clocking state is realized through a stationary magnetization state ($d\mathbf{M}/dt = 0$) of the cell when the magnetization of the free layer is oriented along the y-direction (see Fig. 1(d)). It will be shown theoretically in the next section that such a clocking would require the reference layer to be tilted at 45° to the z-axis (out-of-plane) and to lie in the x-z plane (see Fig. 1(c)). The in-plane magnetization component of the reference layer provides sufficient TMR to successfully read the cell, while at



(a) Through metal layers (b) Through MOS transistor

Fig. 2: Methods of feeding current to Multi-Layer Cells. **(a) Using metal layers** $Metal1$ *and* $Metal2$**:** Positive current I_+ beyond a certain critical value, with electrons flowing from the free layer to the reference layer, can switch the cell to the logic '1' state (position B). Negative flowing current can switch the cell to the logic '0' state (position A). **(b) Through MOS transistor:** The cell is sandwiched between $Metal1$ and the MOS transistor, that feeds current to the cell. Switch to the logic '0' state through a negative flowing current I_-, beyond a critical or threshold value, is shown.

the same time offers much less coupling onto the free layer so that the neighbor interaction dominates in deciding the cell's state.

IV. Key device parameter derivation

As discussed above, multi-layer devices can be switched between their two logic states using STT current. They can also be suitably clocked using STT current for specific device configurations. TMR between the logic states for certain device models can be used to read the device state through integration with a CMOS readout circuitry. In the following subsections we delve into a theoretical approach for the critical current estimation in switching, clocking and in effective TMR calculation between the logic states of the tilted-polarizer reference layer cell.

A. Switching Current Calculation

The current driven switching in the multi-layer devices occurs through a transfer of momentum between the spin-polarized electrons constituting the current and those building up the device magnetization. Depending on the current polarity, the spin-induced torque either opposes or favors the torque induced by the damping component (see Eq. (2)). For a multi-layer structure with tilted-polarizer reference layer and an inplane polarized free layer, the switching can occur either through multiple precession oscillations or through a single 180° rotation of the magnetization of the free layer depending on the magnitude and duration of the current pulse [32]. Precession oscillations occur when the magnetization relaxes through several concentric trajectories before aligning with the energy minimum direction. We have calculated the current requirements for a single precession magnetization reversal of the device under examination. As pointed out by Kent et al. in [32], the spin torque represented by $\hat{m} \times (\hat{m} \times \hat{m_p})$ causes the magnetization of the free layer to rotate out-of-plane. For a switch from logic '1' to logic '0', a positive current pulse followed by a negative one of appropriate durations is required to bring the free layer magnetization along '+x' direction after a traversal through an out-of-plane trajectory. The time of switching would be in the order of $T \approx 1/(4\gamma \mathrm{M})$ where γ is the gyromagnetic ratio and M is the magnetization of the free layer. The influence of the tilted polarizer reference layer on the free layer can be rightfully included by the factor of $1/\sqrt{2}$ to $\mathbf{H_{eff}}$ in the switching current equation [35] of an Inplane Cell. The critical current for switching is therefore given by

$$|I_c| = \left(\frac{2e}{\hbar}\right) \cdot \left[\frac{\alpha M_s . Vol}{\eta(\theta)}\right] . \mu_0 \left(H_k + \frac{H_{eff}}{2\sqrt{2}}\right) \tag{5}$$

where

$$\eta(\theta) = \frac{p}{1 \pm p^2} \qquad p = \sqrt{(TMR/(TMR+2))} \tag{6}$$

$\pm$ is for switch from $logic\ 0 \rightarrow logic\ 1$ and vice versa.

$$H_{eff} = 4\pi M_s \gg H_k \tag{7}$$

The critical current pulse duration, t_d, for switching can be approximated by [32]

$$t_d = \frac{1}{4\gamma M} \tag{8}$$

Note that all the symbols used in equations are defined in Table II. For low energy applications the switching can be effected using a single polarity pulse of shorter duration ($\leq t_d/2$), but the magnetization is left to precess through several oscillations before settling to the final state.

B. Clocking Current Estimation

According to spin-torque induced clocking, the clocking is performed by using appropriate current to drive the cell to a stationary magnetization state along the y-axis. The clocking current can therefore be theoretically derived from Eq. (2) by substituting d**m**/dt = 0 (stationary) and equating the field components along the $\hat{x}$, $\hat{y}$ and $\hat{z}$ directions. The coupling from the underneath tilted reference layer is brought about by the addition of the field term H_d to H_{eff} where H_d is given by

$$\mathbf{H_d} = -H_{dx}\hat{e_x} + H_{dz}\hat{e_z} = -H_d\alpha_p\hat{e_x} + H_d\gamma_p\hat{e_z} \tag{9}$$

$\mathbf{H_{eff}}$ is given by [29]

$$\mathbf{H_{eff}} = \mathbf{H_d} + \mathbf{H_M} + \mathbf{H_{AN}} \tag{10}$$

where H_M being the field due to demagnetization effects and H_{AN} arising out of the crystalline and shape anisotropy of the free layer. During the clocking state H_{AN} = 0 and H_M = -$D_y.M_y.\hat{e_y}$ owing to the presence of only the y-component of magnetization. Also from the fundamental constraint,

$$|\mathbf{M}(\mathbf{r}, t)| = M_s \tag{11}$$

in the clocking state we have

$$M_y = M_s \tag{12}$$

Therefore, when clocked, Eq. (2) modifies to

$$\gamma M_s \hat{m} \times \hat{h_{eff}} = \gamma M_s \frac{J_e}{J_p} G \hat{m} \times \hat{e_p} \times \hat{m} \tag{13}$$

where

$$m = \hat{e_y} \tag{14a}$$

$$h_{eff} = \frac{1}{M_s}\left[-H_{dx}\hat{e_x} - D_y M_s \hat{e_y} + H_{dz}\hat{e_z}\right] \tag{14b}$$

Equating the $\hat{e_z}$ and $\hat{e_x}$ terms gives

$$M_y\left(\frac{J_eG}{J_p}\right) = \frac{H_{dx}}{\gamma_p} \tag{15a}$$

$$M_y\left(\frac{J_eG}{J_p}\right) = \frac{H_{dz}}{\alpha_p} \tag{15b}$$

which mandates

$$\alpha_p = \gamma_p \tag{16}$$

i.e. the reference layer should have a tilt of 45° in its polarization with the z-axis. Therefore, the device switches to a clocked state with a current density of (See Table II for symbol definitions)

$$J_e = \left(\frac{\mu_0 \cdot M_s \cdot \mid e \mid \cdot d \cdot H_d}{\hbar \cdot G}\right) \tag{17}$$

C. TMR Estimation

A 45° tilt in the polarization of the reference layer provides sufficient magnetization component along the x-axis or the easy axis of the free layer. This inplane magnetization component gives the structure the sought-after TMR between its two logic states, enabling an on-chip CMOS readout circuit facility for the device. Here we concentrate on deducing the theoretical TMR estimation from existing literature.

The conductivity of the multi-layer device is given by [36]

$$G(\theta) = \frac{1}{2}(1 + cos(\theta))G_p + \frac{1}{2}(1 - cos(\theta))G_{ap} \tag{18}$$

θ varies with current according to [37]

$$\theta \sim cos^{-1}\left[\frac{H_{dz} - \left(\frac{\hbar}{2e\alpha}\right)\left[\frac{g(\pi/2)}{M_s \cdot Vol}\right] I}{4\pi M_s + (H_k \pm H_{dx})/2}\right] \tag{19}$$

If G_0 and G_1 refers to the conductances of the device during the logic '0' and logic '1' states respectively (refer Figs. 2(a) & 2(b)), then

$$G_0 = \frac{1}{2}(1 + cos(\theta_0))G_p + \frac{1}{2}(1 - cos(\theta_0))G_{ap} \tag{20a}$$

$$G_1 = \frac{1}{2}(1 + cos(\theta_1))G_p + \frac{1}{2}(1 - cos(\theta_1))G_{ap} \tag{20b}$$

where

$$\theta_0 = 45^\circ \qquad \theta_1 = 180^\circ - 45^\circ \tag{21}$$

The TMR can then be obtained from the above equations through

$$TMR = \frac{G_1^{-1} - G_0^{-1}}{G_0^{-1}} \tag{22}$$

V. Elemental Cell Modeling

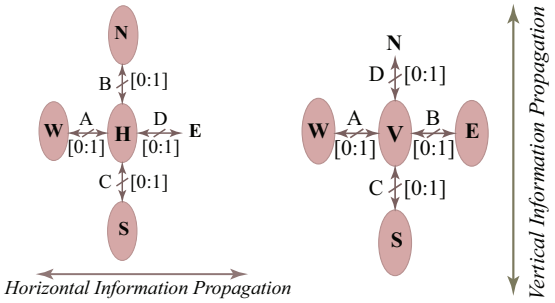
We have emulated the multi-layer cell behavior in Verilog-A and have simulated it in Cadence environment. The Verilog-A code can be downloaded from Modelfiles. In the following two subsections, we discuss the modeled device parameters and the algorithm for modeling neighbor interaction between the multi-layer cells

A. Device Characteristics Modeling

In order to emulate the theoretical cell behavior, we have coded Eqs. (5), (8) and (17) that describe the critical switching current, clocking current density, and critical pulse width respectively, in Verilog-A. The resistance dependence of the device as a function of the current is simulated by incorporating Eqs. (18) & (19) in the model. The intrinsic device parameters used in the model are kept consistent with the values available in literature and are outlined in Table III.

Algorithm 1 Horizontal cell behavior

if A **and** B **and** $C = clocked$ **then**
  $D = U$ {U is undecided state}
else if A **and** $B = clocked$ **then**
  $D = C$
else if A **and** $C = clocked$ **then**
  $D = B$
else if $A = clocked$ **then**
  if $B = C$ **then**
    $D = B$ **and** C {B and C are in same logic states}
  else
    $D = U$
  end if
else if B **and** $C = clocked$ **then**
  $D =$ **not**A
else if $B = clocked$ **then**
  $D = C$
else if $C = clocked$ **then**
  $D = B$
else
  $D = B$ **and** C + (**not**A) **and** (B **xor** C)
end if



(a) Horizontal Cell (b) Vertical Cell

Fig. 3: Modeling neighbor interaction in a Horizontal and Vertical Cell.**(a) Horizontal Cell H** and **(b) Vertical Cell V : N**, **W** , **S** and **E** represents the neighbors along the North, West, South and East direction. A, B, C and D are virtual dual bi-directional magnetic ports that helps to communicate the state of a cell with that of its neighbor.

B. Neighbor Interaction Modeling

We have employed a Finite State Machine to model the cell behavior under the influence of its neighbors. An extension of the observation [38] that ferromagnetic coupling between vertical arrays of single-domain nanomagnetic cells exceeds the antiferromagnetic coupling that binds the cells in a horizontal array for the same vertical and horizontal pitches, is used to emulate the behavior of a multi-layer cell in the association of its neighbors. To personate the cell behavior in a horizontal and in a vertical array, we have developed two models of multi-layer cells – **the horizontal cell** and **the vertical cell**. While we have maintained identical stand-alone behaviors of the two models, the horizontal cell is used in a horizontal array to propagate information via anti-ferromagnetic coupling and the vertical cell is used in a vertical array and operates under ferromagnetic coupling. The cell behaviors are however identical when used with three active neighbors in a majority logic environment.

Fig. 3(a) shows a horizontal cell under the influence of three immediate neighbors placed to its north, west and south while the cell in itself influences the neighbor to its east. Each cell apart from its two electrical inout ports labeled *rf* – the

TABLE III: Device parameters used in simulation

Device Parameter	Values
Dimension *(L×W×d)*	$100\times50\times2\ nm^3$
Ref. Layer coupling field, H_d	$5000A/m$
Damping constant, α	0.01
Saturation Magnetization, M_s	$8e5A/m$
Spin-polarizing factor, P	0.4
Anisotropy field, H_k	$10Oe$

free layer terminal and *rp* – the reference layer terminal, has four magnetic ports, one on each side. The magnetic ports, A, B, C, and D, are virtual bi-directional dual ports that we have designed to either collect information about the state of a neighbor or to inform an immediate neighbor about the state of the cell. The underlying assumption that we employed in the designing of the model is that the magnetostatic interaction from immediate neighbors — to the north, west, south and east of a cell are only able to influence its state and that a cell has no influence from neighbors located further away. The states of a cell are defined as: *Logic '1'*-'11', *Logic '0'*-'00' and *Clocked*-'01'.

Fig. 3(b) shows a vertical cell with neighbors to its west, south and east. Algorithms 1 and 2 determines the behavior of a horizontal and a vertical cell, respectively, right after they are clocked. The algorithm involves bitwise operation of the magnetic ports. We have implemented the algorithm using a Finite State Machine (FSM).

Algorithm 2 Vertical cell behavior

if A **and** B **and** $C = clocked$ **then**
  $D = U$
else if A **and** $B = clocked$ **then**
  $D = C$
else if A **and** $C = clocked$ **then**
  $D =$ **not** B
else if $A = clocked$ **then**
  $D = C$
else if B **and** $C = clocked$ **then**
  $D =$ **not**A
else if $B = clocked$ **then**
  $D = C$
else if $C = clocked$ **then**
  if $A = B$ **then**
    $D =$ **not** A {A and B are in same logic states}
  else
    $D = U$
  end if
else
  $D = C$ **and** (**not** B) + (**not**A) **and** ((**not** B) **or** C)
end if

The model is generic and is able to simulate the behavior of the cell under any association of neighbors. The absence of a neighbor is emulated by pinning the relevant magnetic port to '01'. A horizontal wire and a vertical wire is simulated by cascading horizontal and vertical cells respectively. For horizontal cells that build up a horizontal wire, the ports B and C are connected to '01' respectively to indicate the absence of neighbors in those directions. Similarly for vertical cells in a vertical wire, the effect of ports A and B on each of the cells' V are invalidated by connecting them to '01' respectively. Thereby, through proper arrangements and interconnections between cells we can realize any logic.

VI. Results and Discussions

The Verilog-A model of the multi-layer device has been simulated using Cadence Spectre for device dimensions of $100 \times 50 \times 2\ nm^3$. The device model has been integrated with $22\ nm$ predictive CMOS technology [39], [40], [41], [42] and the spin-transfer torque switching has been extensively verified.

Table IV states the values of critical currents for switching and clocking, and the average and peak currents during switching *(to both logic '1' and logic '0' states)*. The current magnitudes, so reported, are obtained through simulations of the Verilog-A model in the Cadence environment. Simulation results of the switch to logic '1' and logic '0' states are shown in Fig. 4(a) & 4(b) respectively. The clocking of the device has been thoroughly tested using STT current under circuit configurations shown in Fig. 2(a). The post clocking neighbor influence for neighbor combinations: *N-logic '0', W-logic '1' and S-logic '1'* are shown in Fig. 5.

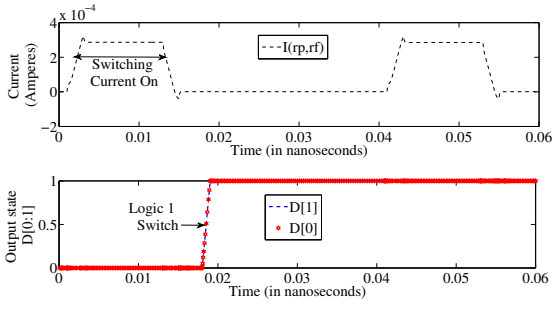
The energy consumed during switching and clocking are mentioned in Table IV. The values obtained clearly shows an improvement in power consumption over field-induced clocking where current in the order of mA is required to flow through the top or bottom wires to produce the required magnetic field. The clocking frequency for field-induced clocking is $10^8\ Hz$ with 50% duty cycle and a clocking current of $4mA$ [20]. For the planar cell dimensions of $100 \times 50\ nm^2$ and a pitch of $120\ nm$, field-induced clocking of $>11,000$ cells would require a clock wire length of $\approx 1.412\ mm$ with an overall resistance of $63.54\ \Omega$. Since the clocking in STT current-induced clocking is implemented using a stationary state in the y-axis, the clocking duration can be fairly approximated to be $10\ ps$ for a clocking current of $170\ \mu A$. From Fig.6, it is evident that STT current-induced clocking is more effective in energy consumption for up to $11,765$ cells being clocked in the same clocking cycle.

As mentioned by Niemier et al. in [20], the underneath wire of $2\mu m$ wide by $0.2\ \mu m$ thick by 4μm long was used to clock a line of cells. Such a clocking scheme would be suitable to clock a long interconnect. For our cell size of $100\times50\times2\ nm^3$, such a clocking wire can clock approx. 32 cells that are ferromagnetically coupled while maintaining a pitch of $120\ nm$. However, if the cells in two such adjacent clock zones need to interact to realize any fundamental Boolean logic like majority AND or OR, the clocking scheme fails since the minimum separation between the adjacent cells *(equal to the wire width of* $2\ \mu m$*)* is well beyond the maximum permissible separation between the cells over which they interact.

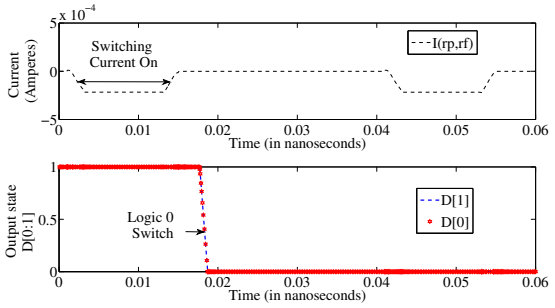
For a fully parallel *(θ = 0°)* and anti-parallel (θ = 180°) conductance of (G_p = $2.82\times10^{-3}\ mho$) and (G_{ap} = $1.967\times10^{-3}\ mho$) respectively [36], a TMR of 28.83% is obtained with this device architecture. This TMR is sufficient enough to read the cell's state correctly using a CMOS read-out circuitry. Therefore, such a multi-layer device, with STT current-induced switching, clocking and a TMR distinguishing the two binary logic states, is capable of building MQCA logic with on-chip input, clock and output circuitry. Moreover, as seen from Eqs. (5) & (17), as the device scales down, the

TABLE IV: Single cell critical current, critical pulse duration, average current and critical energy consumption in STT current-induced switching and clocking approach. The critical currents are obtained from Eqs. (5) & (17). The average current is obtained from the simulations of the Verilog-A model in Cadence using a current pulse period of 40 ps with an 'On' duration equal to the critical pulse duration as shown in Figs. 4 & 5. Such current pulses are justified for low energy applications [32].

Operation	Critical Current I_c (μA)	Critical Current pulse duration $t_d/2$ [32]	Average Current I_{avg} (μA)	Energy consumed during switching E_c=$I_c \times t_d/2$
Switch to logic '1' from logic '0'	278.9	≈10 ps	109.4	2.789 fJ
Switch to logic '0' from initial logic '1'	-216	≈10 ps	85	2.16 fJ
Clocked State *(+y direction)*	169.3	≈10 ps	68.435	1.693 fJ



(a) Switching to logic '1' State from initial logic '0' state



(b) Switching to logic '0' State from initial logic '1' state

Fig. 4: STT current induced switching of the cell. (a) Switch to logic '1' state from initial logic '0' state through spin-torque transfer effect from positive current. The transistor dimension used is $194nm/22nm$. (b) Switch to logic '0' state from initial logic '1' state through negative current. The transistor dimension used is $130nm/22nm$.

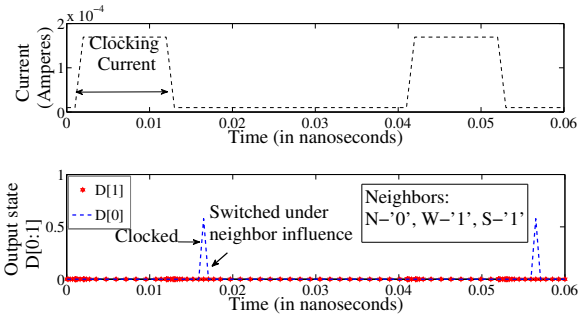


Fig. 5: STT current-induced clocking and post-clocking neighbor influence on a Horizontal Cell. Neighbor states: **N** *(logic '0')*, **W** *(logic '1')*, **S** *(logic '1')*.

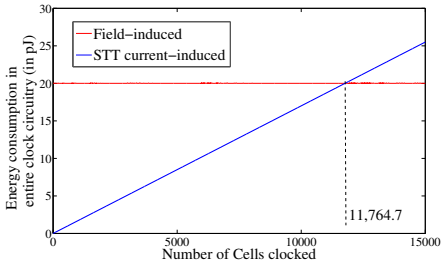


Fig. 6: Energy consumption in the clocking operation ($I_{clk} \cdot V_{dd} \cdot t_{clk}$) vs. number of cells in STT current-induced clocking (170 μA [32]) and Field-induced clocking. The clocking frequency for Field-induced clocking is 10^8 Hz with 50% duty cycle with a clocking current of 4 mA [20]. For the planar cell dimensions of 100×50 nm^2 and a pitch of 120 nm, field-induced clocking of $11,765$ cells would require a clock wire length of 1.412 mm with an overall resistance of 63.54 Ω.

current required for switching and clocking also scales down in proportion to the volume, making them ideal for targeting low power applications.

In addition, the effect of stray magnetic fields on the free layer of a cell is calculated. The fields originate from the free and reference layers of neighboring cells, bit and source lines of its own and neighboring rows of cells and from its own reference layer. For the above cell dimensions and an inter cell spacing of $20nm$ along both horizontal and vertical direction, the stray fields magnitudes have been $\ll 75Oe$ [43], which is required to switch a cell's state under room temperature.

VII. Conclusion

We have extended the existing MQCA implementation ideologies to target low power applications. The half-precession switch of the multi-layer cells paves the way for ultra-fast logic development. This is the first work to report MQCA logic with individual controllability over logic elements due to STT current-induced switching and clocking. The multi-layer devices used for logic implementation eliminate the overhead in cost arising from fabrication of current-carrying wires that initially provided the requisite magnetic fields for switching. The multi-layer cells facilitate integration with CMOS technology which enables the development of on-chip readout circuitry. The tilted-polarizer reference layer cells provide sufficient TMR for an effective readout operation while at the same time providing low current clocking strategy and post clocking neighbor interaction. We have developed a Verilog-A model emulating the necessary behaviors, primary cell characteristics and neighbor interactions, that is the key to simulating the proposed MQCA cell with CMOS circuitry. Thus, in this paper we have put forward a new dimension to the existing MQCA architecture that enables future developments of ultra-fast low power logic blocks.

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Jayita Das received her Bachelors degree in Electronics and Communication Engineering from National Institute of Technology, Durgapur, India in 2004. She has worked as Scientist in Defense Research Development Organization, India in the field of VLSI Design. She is currently pursuing her PhD in the Department of Electrical Engineering, University of South Florida. Her primary research interests are in nanomagnetic logic, device modeling, stochastic computing. She is the recipient of the USF Presidential Doctoral Fellowship.

Syed M. Alam (M' 04) received his B.S. degree in electrical engineering from the University of Texas at Austin in 1999, and the S.M. and Ph.D. degrees in electrical engineering and computer science from Massachusetts Institute of Technology in 2001 and 2004, respectively. He is currently a Senior Member of Technical Staff at Everspin Technologies (a start-up from Freescale Semiconductor) working on research and development for various design aspects of standalone and embedded MRAM. His expertise and research interests include emerging memory design and test, 3D integration technology, thermal analysis, and signal integrity. He has over 40 publications in refereed journals and conferences, and holds four US patents with eight more pending on the above areas. He presented several invited talks including tutorials at ISQED, ICCAD, and GLSVLSI. Dr. Alam has served on the technical program committees of DAC, ISQED, ICCAD, GLSVLSI, ISVLSI, and on the Computer Architecture panel for National Science Foundation. He is a member of Sigma Xi Scientific Research Society.

Sanjukta Bhanja received her Bachelor degree in electrical engineering from Jadavpur University (1991) Calcutta, her Masters from Indian Institute of Science (1994), Bangalore, India and Ph.D. in computer science and engineering from University of South Florida (USF), Tampa in 2002. She is currently an Associate Professor with the Department of Electrical Engineering, USF. Her primary research interest is in non-CMOS nano-computing, exploring novel state variables, alternate computing paradigm with heterogeneous devices. Dr. Bhanja is an Associate Editor of the IEEE TVLSI. She has served on the Technical Program Committee of various IEEE and ACM conferences. She is currently the Emerging Technology track co-chair in IEEE DATE11 and has served as Technical Program Co-Chair of IEEE ISVLSI, ACM GLSVLSI and as General Co-Chair of ACM GLSVLSI. She is a recipient of NSF CAREER Award (20072012), USF Tau Beta Pi Outstanding Engineering Faculty Researcher Award in 2007, USF 2008 Outstanding Faculty Research Achievement Award, 2010 Florida Education Foundation (F.E.F) William Jones Outstanding Mentor Award, and USF 09/10 Outstanding Undergraduate Teaching Award.